IN THE SPECIFICATION

Please amend the specification as follows:

Please replace paragraph **[0005]** with the following:

[0005] According to an aspect of the present invention, there is provided apparatus for rendering animated image data in real time, comprising: central processing means, data storage means, graphical processing means, and texture storage means, said data storage means for storing data including scene data, that defines a plurality of sequentially displayable scenes, each of which will be rendered as an image sequence in real time; data for each said scene including a texture for the respective scene, that requires transfer to said texture storage means in advance of its rendering; said central processing means and said graphical processing means being configurable to perform operations to render said scenes, without a pause between scenes, said operations being under control of said central processing means, which is configurable to execute instructions for performing steps of: (a) rendering the next frame of the current scene; (b) estimating a bandwidth availability for texture transfer that is unlikely to interfere with real-time rendering of the current scene; (c) identifying the amount of data in a texture required for rendering a next scene; (d) splitting said required texture into texture portions that satisfy said bandwidth availability; and (e) transferring a said texture portion from said data storage means to said texture storage means.

Please replace paragraph **[0027]** with the following:

[0027] Examples of combined animation and camera broadcast images are shown in *Figures 3* to *6*. Most of these scenes are simple, having mainly two-dimensional animations. However, the animation application instructions are capable of generating fully three dimensional animated images in real time. In *Figure 3*, a news reader **104** occupies the central part of the screen. Several animations are super-imposed upon the camera image, as shown at **301**, **302**, **303**, **304** and **305**. These may be updated from frame to frame as the live broadcast proceeds.

Please replace paragraph **[0034]** with the following:

[0034] The processing system **101** shown in *Figure 1* is detailed in *Figure 8*. The processing system **101** comprises two central processing units **801** and **802** operating in parallel. Each of these processors is an MIPS R12000 manufactured by MIPS Technologies Incorporated, of Mountain View, California. Each of these processors **801** and **802** has a dedicated secondary cache memory **803** and **804** that facilitate per-CPU storage of frequently used instructions and data. Each CPU **801** and **802** further includes separate primary instruction and data cache memory circuits on the same chip, thereby facilitating a further level of processing improvement. A memory controller **805** provides a common connection between the processors **801** and **802** and a main memory **806**. The main memory **806** comprises two gigabytes of dynamic RAM.

Please replace paragraph **[0042]** with the following:

[0042] It is possible that, during a particular live broadcast, there will be a break between scenes, which would enable an operator to choose new scenes to download. However, this would be very unsatisfactory. In practice, therefore, it will be necessary to preload new scenes while a[[n]] current scene is being rendered. Preloading for a new scene will, by necessity, include the preloading of texture memory **809** with the textures for the new scene.

Please replace paragraph **[0046]** with the following:

[0046] In the 5mS assumed to be available, a total of 125Kbytes can be transferred, which is only half of the texture. Furthermore, the 5mS figure is just a guess. In reality, the available bandwidth [[is]] varies dramatically. Sometimes practically no bandwidth is available at all.

Please replace paragraph **[0050]** with the following:

[0050] Data that defines each of four scenes is shown at **911, 912, 913** and **914**, along with respective textures **921, 922, 923** and **924**. Statistics **931** include data for predicting the available bandwidth for texture transfer; without violating the requirement for real time rendering. Other data includes data structures and storage used by various components of the operating system **901**, as well as the application instructions **902**.

Please replace paragraph **[0057]** with the following:

[0057] At step **1302** the bandwidth availability is estimated. At step **1303** a question is asked as to whether any textures are required to be pre-loaded into texture memory. If so, control is directed to step **1304**. Alternatively, control is directed to step **1309**. At step **1304** a question is asked as to whether a texture portion is already available for pre-loading. If so, control is directed to step **1305**. Alternatively, control is directed to step **1306**. At step **1305** a question is asked as to whether the next portion can be pre-loaded now. This is evaluated according to whether the texture portion can be transferred within the available time before the next frame is required. This evaluation is performed by comparing the size of the texture portion with the estimate provided at step **1302**. If there is insufficient transfer bandwidth available, control is directed to step **1309**, and the portion will have to be pre-loaded during a subsequent frame. Alternatively, control is directed to step **1308**, where texture pre-loading takes place.

Please replace paragraph **[0061]** with the following:

[0061] A graph of the processing load which occurs over a period of several frames is shown in *Figure 15*. Each frame has a period of approximately 16.67mS in which to be rendered, after which front and back buffers in the graphics card **808** are swapped, thus making the newly drawn animation frame visible. The amount of time taken by the central processing units **801** and **802** to render a frame is variable, resulting in a variable amount of free time **1501, 1502, 1503** and **1504** in which texture transfer, and other background operations[[,]] can be performed.